REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated November 30, 2005 (U.S. Patent Office Paper No. 11272005). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1-8 stand for consideration in this application, wherein claim 3 is being canceled without prejudice or disclaimer, while claims 1 and 6 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. All amendments to the application are fully supported therein, including page 16, line 10 – page 17, line 16. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formal Objections

Claim 1 was objected to because the term "element isolation grooves reaching the isolation layer" was unclear as to the meaning.

Claim 3 was objected to because the terms "the plurality of the first bipolar transistors function as a singular bipolar transistor" including "the singular bipolar transistor" was unclear as to the meaning.

Claim 1 is being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. As mentioned above, claim 3 is being cancelled, and therefore the rejection of claim 3 is moot. Accordingly, withdrawal of this objection is respectfully requested.

Prior Art Rejections

The First 35 U.S.C. §102(b) rejection

Claims 1-8 were rejected under 35 U.S.C. §102(b) as being anticipated by Uchida et al. (Pat. No. 5214302) (hereinafter Uchida '302). As mentioned above, claim 3 is being cancelled, and therefore the rejection of claim 3 is moot. Applicants respectfully traverse the rejection of claim 1-2 and 4-8 for the reasons set forth below.

According to the M.P.E.P. §2131, a claim is anticipated under 35 U.S.C. §102 (a), (b), and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior reference.

Claim 1

The Office Action contends that Uchida '302 teaches a method comprising: a silicon-on-insulator substrate including a base substrate, an insulating layer over the base substrate, and a semiconductor layer over the insulating layer; electric circuit formed over the silicon-on-insulator substrate; a plurality of semiconductor islands used as element-forming regions in a first area of the silicon-on-insulator substrate; and a plurality of first bipolar transistors formed in the respective semiconductor islands, and each respectively having an emitter region, a base region, and a collector region formed in the semiconductor layer; wherein the plurality of semiconductor islands are isolated each other by element isolation grooves reaching the isolation layer of the silicon-on-insulator substrate; and the emitter regions, the base regions, and the collector regions of the plurality of the first bipolar transistors are electrically connected by interconnection wirings respectively. Applicants respectfully disagree.

Uchida '302 shows a semiconductor integrated circuit device having a structure in which a first region for forming the base and emitter regions of each of bipolar transistors and a third region for forming each of the MISFETs, is projected from the main surface of a semiconductor substrate. Uchida shows that the base region and the emitter regions of the bipolar transistor are electrically and self-alignedly connected to a base electrode. However, Uchida '302 does not expressly or implicitly teach that the base region and the emitter regions of the bipolar transistor are parallel-connected.

In contrast, the present invention as recited in amended claim 1 provides that the emitter regions, the base regions, and the collector regions of the plurality of the first bipolar transistors are electrically parallel-connected by interconnection wirings respectively to act simultaneously and act as a large transistor. Since a large size of a transistor can be configured by the present invention, degradation of characteristics of a base resistance and other circuit parameters can be avoided. Furthermore, heat radiated from large current transistors can be dissipated through the wirings of the parallel connection because a transfer rate of the heat in a silicon-on-insulator semiconductor device is significantly lowered. Since

Uchida '302 does not have parallel connected wirings, Uchida '302 does not have such an effect.

Therefore, Uchida '302 does not show every element recited in amended claim 1. Accordingly, claim 1 is not anticipated by Uchida '302.

Claims 2, 4-5

As to dependent claims 2 and 4-5, the arguments set forth above with respect to independent claim 1 are equally applicable here. The base claim being allowable, claims 2 and 4-5 must also be allowable.

Claim 6

Claim 6 has the substantially same features as those of claim 1. As such, the arguments set forth above are equally applicable here. Claim 1 being allowable, claim 6 must also be allowable.

Claim 7-8

As to dependent claims 7-8, the arguments set forth above with respect to independent claim 6 are equally applicable here. The base claim being allowable, claims 7-8 must also be allowable.

The Second 35 U.S.C. §102(b) rejection

Claims 1-8 were rejected under 35 U.S.C. §102(b) as being anticipated by Uchida et al. (Pat. No. 4746963) (hereinafter Uchida '963). As mentioned above, claim 3 is being cancelled, and therefore the rejection of claim 3 is moot. Applicants respectfully traverse the rejection of claim 1-2 and 4-8 for the reasons set forth below.

Claim 1

The Office Action contends that Uchida '963 teaches a method comprising: a silicon-on-insulator substrate including a base substrate, an insulating layer over the base substrate, and a semiconductor layer over the insulating layer; electric circuit formed over the silicon-on-insulator substrate; a plurality of semiconductor islands used as element-forming regions in a first area of the silicon-on-insulator substrate; and a plurality of first bipolar transistors formed in the respective semiconductor islands, and having respective an emitter region, a

base region, and a collector region formed in the semiconductor layer; wherein the plurality of semiconductor islands are isolated each other by element isolation grooves reaching the isolation layer of the silicon-on-insulator substrate; and the emitter regions, the base regions, and the collector regions of the plurality of the first bipolar transistors are electrically connected by interconnection wirings respectively. Applicants respectfully disagree.

Uchida '963 shows a semiconductor device wherein an isolation area is a region in which a burying material is buried in a deep groove formed in a semiconductor body. As well as Uchida '302, Uchida '963 does not expressly or implicitly teach that the base region and the emitter regions of the bipolar transistor are parallel-connected. Therefore, the arguments set forth above are equally applicable here. That is, Uchida '302 does not show every element recited in amended claim 1. Accordingly, claim 1 is not anticipated by Uchida '963.

Claims 2, 4-5

As to dependent claims 2 and 4-5, the arguments set forth above with respect to independent claim 1 are equally applicable here. The base claim being allowable, claims 2 and 4-5 must also be allowable.

Claim 6

Claim 6 has the substantially same features as those of claim 1. As such, the arguments set forth above are equally applicable here. Claim 1 being allowable, claim 6 must also be allowable.

Claim 7-8

As to dependent claims 7-8, the arguments set forth above with respect to independent claim 6 are equally applicable here. The base claim being allowable, claims 7-8 must also be allowable.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor

rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

April 26, 2006